Active Frequency-Multiplier Design Using CAD

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***Abstract*—A tutorial paper on active frequency multiplier design is presented. Rough calculations for a $\times 2$ multiplier using classical theory are developed and used as a starting point for implementation with nonlinear computer-aided design (CAD) software. The power of the nonlinear CAD software for visualizing and understanding concepts important to frequency multiplier design, and also for optimization of critical design parameters is demonstrated through realistic example. Important design considerations for higher order multipliers are discussed, including design of output termination circuitry for a $\times 4$ multiplier at 28 GHz.**

***Index Terms*—Active multiplier, computer-aided design (CAD) software, FET multiplier, frequency multiplier, harmonic balance (HB), harmonic terminations, high-order multiplier, nonlinear, optimization, tutorial.**

I. Introduction

THERE IS currently an explosion in wireless communication systems under development at upper microwave and millimeter-wave frequencies. Applications above 20 GHz include local multipoint distribution systems (LMDS) at 28 and 40 GHz, satellite systems at 30 GHz, and high-altitude long-operation (HALO) platforms at 47 GHz [1]. Simple effective methods of generating signals at these frequencies are extremely important in the design of cost-effective transceiver circuits.

Frequency multipliers are great circuits for generating signals, providing much signal-processing functionality with very simple circuitry. As such, they are especially suitable for realizing highly integrated hardware solutions for emerging applications at upper microwave and millimeter-wave frequencies, including not only generation of frequency-stable reference signals, but also modulation and frequency translation [2][3].

"High order" multipliers (i.e., $\times 3$ or higher) can be fairly difficult to design for good performance and many tradeoffs must be explored. Diodes have been traditionally employed for implementation of high-order frequency multipliers [4]. Diode multipliers, however, are often unsuitable for current applications, as they require high input drive levels and have high conversion loss. Comparably, active frequency multipliers require low input levels, have high conversion efficiencies, and can provide conversion gain, making them very attractive for highly integrated planer circuit solutions and monolithic microwave integrated circuits (MMICs) [5]. Active multipliers with orders as high as $\times 5$ [6] and $\times 7$ [7] are generally realizable with a single FET stage. For higher order multipliers, cascading of stages is usually more effective. For example, a $\times 12$ multiplier can be realized at 28 GHz by cascading two FET stages [8].

This paper is a tutorial on active frequency multiplier design using nonlinear computer-aided design (CAD) software. The power of the CAD software for visualizing and understanding the nonlinear effects prevalent in FET multipliers, and also for optimizing critical design parameters, is demonstrated through realistic example. In particular, a $\times 2$ multiplier at 12 GHz is chosen for the main tutorial presentation. The $\times 2$ stage provides a strong second-order nonlinearity, compared to a higher order multiplier with comparatively weak nonlinear characteristics, which are easily masked by the much stronger lower order nonlinear effects. The $\times 2$ stage, therefore, is more suitable for tutorial presentation since the nonlinear effects can be more readily observed with the CAD software and the important concepts and tradeoffs more easily explained. Following the main tutorial presentation, some important design considerations for high-order multipliers are discussed and the design of a $\times 4$ 28-GHz multiplier output circuit is presented.

The tutorial begins with "rough" calculations based on classic theory. Maas [9] gives an excellent treatment of this theory so it is only briefly discussed here and demonstrated through example. The rough design parameters are used as a starting point for nonlinear CAD design and optimization. The package used for the tutorial is *Agilent Advanced Design System* (*ADS*),[1] but the method presented is suitable for use with most CAD packages supporting nonlinear transistor models, harmonic balance (HB) as the nonlinear engine, and optimization routines. The *ADS* design files are included with this tutorial and can be run in parallel with *ADS* version 1.3 or higher. For those without access to *ADS*, the tutorial has been designed with "hyperlinks" to embedded *ADS* schematics and results at various stages of the tutorial, to give the reader the "feel" of the CAD design and simulation process. The Adobe Acrobat reader is required to access these features in the portable document file (PDF) version of the tutorial paper. Some of the results and a simplified schematic are also included in the text version of this paper.

II. Background

Frequency multiplication is a process by which a nonlinear circuit is used to generate harmonics of a fundamental frequency input signal. Therefore, rather than attempting to prevent and control the circuit nonlinearity, as with small-signal linear design, this is the feature that is desired and actually enhanced.

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This paper has supplementary downloadable material available at http://ieee-explore.ieee.org, provided by the authors. This paper is a tutorial on active frequency multiplier design using nonlinear CAD software. The paper is best executed in electronic form since the print version does not include the extensive "hyperlinked" material that is available in the electronic version. This material is 2.2 MB in size.

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[1]*ADS*, ver. 1.3, Agilent Technol., Palo Alto, CA.

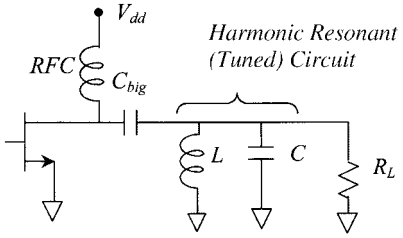

Fig. 1. FET multiplier circuit with harmonic output resonator.

The basic circuit for an FET multiplier is shown in Fig. 1. The FET is biased at a nonlinear operating point to generate high harmonic output distortion. The desired harmonic signal is then selected, while the fundamental frequency and all other harmonic signals are rejected, usually by a narrow-band tuned circuit centered at the desired harmonic frequency. A simple tuned circuit often does not have a sufficient quality factor (Q) to adequately short out the low-order harmonic components, and separate harmonic short-circuit terminations are often employed. This situation is further discussed through example in Sections IV-B and V. A more subtle consequence of the nonlinear circuit response is instantaneous phase multiplication, by the integer harmonic number, which provides interesting possibilities for combining modulation with frequency translation [2], [3].

As a result of the strong nonlinearities, the parameters important for small-signal linear active design (i.e., S-parameters, gammas (Γ's), etc.) are a function of signal level, and are also somewhat ill defined due to the harmonic signals present at the ports. The traditional design procedures for linear design using these parameters are, therefore, not very useful if extended to strongly nonlinear circuits. However, extraction of "large-signal" S-parameters (i.e., to give estimates of input and output Γ's) can be very useful in providing estimates of termination impedances, which can be used as a starting point for nonlinear analysis, design, and optimization using CAD. The use of nonlinear CAD software with accurate nonlinear circuit models is essential for predicting nonlinear behavior and designing realistic multiplier circuits.

A. HB

Most modern CAD packages use some variation of HB as the nonlinear simulation engine, which allows analysis of circuits containing both linear and nonlinear elements excited by large-signal periodic sources. HB is quite mature, and is generally considered accurate and appropriate for the analysis of strongly nonlinear circuits. The technique is not presented here in detail and the reader is referred to Maas [9] for a comprehensive discussion of the technique.

The HB method is based on the principle that, for a sinusoidal excitation, there exists a steady-state solution for the network node voltages and currents that can be approximated using a Fourier series. This solution can be represented as a set of node voltage and current phasors at harmonics of the fundamental excitation frequency. The accuracy of the approximation of the steady-state nonlinear behavior improves as more harmonics of the fundamental excitation are included in the analysis. The circuit is divided into linear and nonlinear subcircuit multiport networks, with each element in the nonlinear subcircuit connected to ports in the linear subcircuit. The premise of the HB is that, if a set of harmonic port voltages gives the same solution, within acceptable error, for the port currents as calculated in both the linear and nonlinear subnetworks, then these port voltages approximate the steady-state solution up to the chosen harmonic with the specified degree of accuracy. The port voltages and corresponding currents for the linear network are calculated first in the frequency domain, using N-port parameter representations and linear-circuit-analysis techniques. An inverse Fourier transform is then performed on the port voltages to obtain the port time voltage waveforms. The currents into the nonlinear elements at the ports are then determined from the port voltage time waveforms and the models for the nonlinear elements. A Fourier transform is then performed on the nonlinear port current time waveforms to convert these to the frequency domain, for comparison with the port currents as calculated by the linear subcircuit. This comparison is the basis for an error function meant to drive a new estimate of the port voltages. This process of estimation is repeated until convergence to a solution is obtained. The availability of circuit node voltages and currents in the time domain, as well as the frequency domain, is a very useful byproduct of the inverse Fourier transform in the HB analysis as these time waveforms are extremely valuable for observing the gate and drain behavior of the FET multiplier.

III. Multiplier Design Example

The first step in the design process is to choose a suitable FET. To get appreciable power out of the multiplier, the FET must be subjected to fairly high maximum drain current and be able to handle high (negative) gate-to-source voltage and high gate-to-drain voltage without breakdown. This generally limits practical use to "medium power" devices. Small drain-to-source capacitance is also desirable for high-frequency operation.

An approximate frequency multiplier design procedure is illustrated by way of example as follows.

> *Design a $\times 2$ frequency multiplier using the NEC NE9000 medium power GaAs FET to deliver maximum power to a real load at 12 GHz. The input frequency is 6 GHz and the output frequency is 12 GHz. Do an approximate design to obtain an estimate of the output termination, conduction angle, gate bias voltage, output power, and power efficiency. Assume a drain bias of $V_{dd} = 5$ V, maximum drain current of $I_{\max} = 100$ mA (at $V_{g,\max} = 0$ V), gate conduction threshold voltage of $V_t = -3.0$ V, drain saturation voltage of $V_{\rm SAT} = 1$ V, and drain-to-source capacitance of $C_{ds} = 0.15$ pF.*

There are a variety of nonlinear mechanisms present in an FET multiplier that can contribute to harmonic generation. These include equivalent-circuit elements such as the gate-to-source capacitance, $C_{\rm gs}$, the transconductance, g_m, and the output conductance, G_d, which are nonlinear functions of signal level (i.e., V_g, V_d) under large-signal excitation. The primary source of the nonlinearity, however, is usually some form of drain current "clipping." This can be achieved by biasing the FET gate such that the drain current clips when either the gate voltage exceeds the forward conduction threshold, or when the gate voltage drops below the "turn-on" threshold voltage V_t.

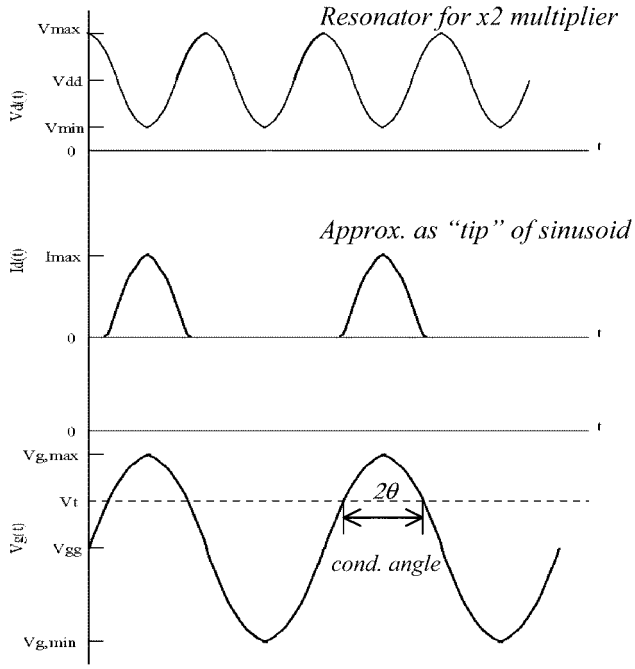

Fig. 2. FET multiplier IV waveforms.

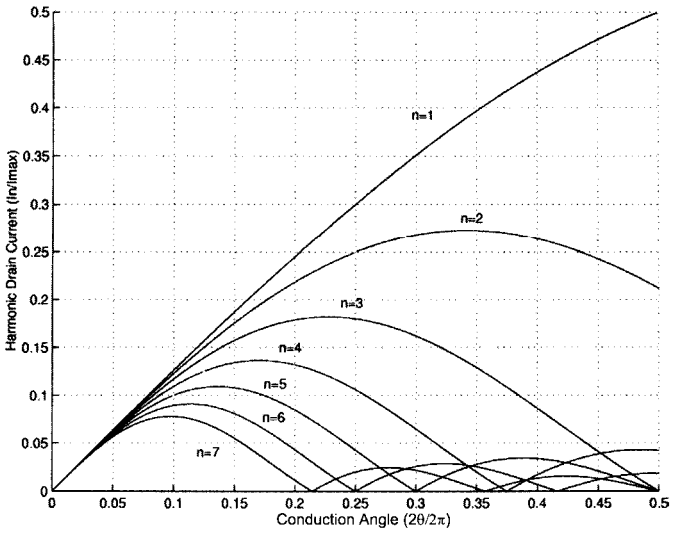

Fig. 3. Ideal harmonic drain current as a function of FET drain conduction angle.

When biased below V_t, the FET is biased at a "Class-C" power amplifier bias point. It has been suggested that the Class-C mode of operation is less prone to device failure [10], and this is the mode considered here.

The conduction angle, shown as 2θ in Fig. 2, is the fraction of the fundamental frequency input signal cycle (360°) for which current flows in the FET drain (i.e., the gate voltage exceeds V_t). With the Class-C bias point, the FET drain conducts for less than one-half of the input cycle (<180°), producing a drain current waveform that is rich in harmonic distortion. A popular model for the drain current waveform is that of a train of half-cosine pulses [9], although this model is only an approximation, as a real FET will exhibit a gradual nonlinear increase in drain current as V_t is exceeded at the gate and the drain begins to conduct (i.e., a "soft" turn-on characteristic at the gate threshold). The soft turn-on characteristic is due to the small device transconductance g_m, near the turn-on threshold, which gradually increases as the gate voltage increases.

The gate voltage and drain current waveforms for a constant transconductance FET multiplier are shown in Fig. 2. The maximum drain current is labeled $I_{\max}$ and corresponds to the maximum gate voltage, $V_{g,\max}$. The gate bias voltage (V_{gg}) and minimum gate voltage $(V_{g,\min})$ are normally below V_t for the Class-C bias point. The FET is essentially a controlled current source and the nonlinear drain current shown in Fig. 2, which is rich in harmonic components, is somewhat independent of the impedance presented to the drain, provided that this impedance is not too large (i.e., cannot generally provide current if open circuited). When all harmonics, except the desired harmonic, of the drain current are short circuited (i.e., by a resonator, as shown in Fig. 1, or by separate short-circuit terminations), only the desired harmonic voltage component can exist at the drain, as shown in Fig. 2. The undesired harmonic drain current components still exist in the circuit, but circulate in low-impedance reactive paths and, thus, do not contribute to output power. The desired harmonic drain current component circulates in a real load, which is set large enough to affect large drain voltage swing and produce output power at the desired harmonic. The drain voltage is biased at V_{dd}, and varies from $V_{\max}$ to $V_{\min}$ in response to the load impedance presented to the desired harmonic component of the drain current. In practice, the minimum value of $V_{\min}$ is usually the saturation voltage of the FET (V_{SAT}). The waveforms are shown in Fig. 2 for a second harmonic output resonator.

The gate input signal level and gate bias voltage are selected to obtain a conduction angle that maximizes the output level of the desired harmonic. An approximation relating the harmonic drain current to the FET conduction angle for the constant transconductance case can be obtained using a Fourier series expansion for an ideal cosine pulse train as [9]

$$I_n \approx I_{\max}\frac{4\theta}{\pi^2}\left|\frac{\cos n\theta}{1-(2n\theta/\pi)^2}\right|, \qquad n \geq 1 \tag{1}$$

and

$$I_{\mathrm{dc}} \approx I_{\max}\frac{2\theta}{\pi^2} \tag{2}$$

where I_n is the drain current for the nth harmonic, I_{dc} is the average value of the drain current, $I_{\max}$ is the maximum drain current, and 2θ is the conduction angle ([9] uses t_o/T to represent the conduction duty cycle of the fundamental input signal). The harmonic drain current relative to the maximum drain current for the constant transconductance case from (1) is plotted in Fig. 3 as a function of conduction angle, for harmonics up to the seventh. In order to maximize the desired harmonic output power, $I_{\max}$ should be as large as possible and θ should be chosen to give high I_n.

For the present example, we wish to maximize the second harmonic drain current component. From Fig. 3, the optimal conduction angle is approximately $0.35(360°) = 126°$, which corresponds to $I_n/I_{\max} = 0.27$. Another possible choice of conduction angle would be 180°, which does not maximize

the second harmonic drain current component, but could simplify the termination circuitry as it eliminates the requirement to short the third harmonic, which is zero at this conduction angle. Assuming that the conduction angle is 126° and that $I_{\max} = 100$ mA (i.e., at $V_{g,\max} = 0$ V, a combined dc plus ac value), then the expected second harmonic drain current is 27-mA peak.

Large second harmonic drain current alone cannot produce high output power and efficiency unless this current circulates in a large enough real load resistance to affect large drain voltage swing. The largest practical drain voltage swing is to $V_{\rm SAT}$ (i.e., $V_{\min}$ in the Fig. 2 drain voltage waveform). The ideal drain voltage waveform shown is entirely second harmonic since all other harmonics are shorted at the drain and circulate in the harmonic short circuit terminations. Without the shorts, the drain voltage would saturate much more easily as a result of the large fundamental. This is part of the "magic" of the multiplier as the harmonic drain voltage swing can be much larger than would otherwise be possible. For the present example with $V_{dd} = 5$ V, and assuming a drain voltage swing to $V_{\rm SAT}$, $V_{d,\rm peak} = (5 - 1) = 4$ V, which requires a real load resistance of $4/0.027 = 150\ \Omega$.

The expected second harmonic output power is

$$P_2 = \frac{I_n^2 R_L}{2} = \frac{(27\ \text{mA})^2 (150)}{2} = 55\ \text{mW} \Rightarrow +17.4\ \text{dBm}. \tag{3}$$

The dc power supplied is

$$P_{\rm dc} = \frac{V_{dd} I_{\max} 2\theta}{\pi^2} = \frac{5\,(100\ \text{mA})\,(0.35)(2\pi)}{\pi^2} = 111\ \text{mW} \tag{4}$$

which gives a dc–RF efficiency $P_2/P_{\rm dc} = 50\%$. The output resonator inductance required to cancel C_{ds} at the second harmonic is

$$\omega L = \frac{1}{\omega C_{ds}} \Rightarrow L = \frac{1}{\left(2\pi(12\ \text{GHz})\right)^2 (0.15\ \text{pF})} = 1.17\ \text{nH}. \tag{5}$$

The Q of this resonant circuit must be high enough to act as the harmonic short circuits, unless separate harmonic short-circuit terminations are employed. Low Q may actually be desirable in the second case since it allows potentially wider band operation.

The gate bias voltage and input voltage level are determined as

$$V_{gg} = \frac{V_t - V_{g,\max}\cos\theta}{1 - \cos\theta} = \frac{-3}{1 - \cos\left(\frac{126}{2}\right)} = -5.5\ \text{V} \tag{6}$$

and since $V_{g,\max} = 0$ V, $V_{g,\rm peak}$ is also equal to 5.5 V. The FET must be rated to withstand peak voltages of 11 V at the gate and 20 V from gate-to-drain (since $V_{\max} = 9$ V).

These rough design parameters can be used as a starting point for the CAD design and optimization presented in Section IV.

IV. Design Example Using CAD

In this section, nonlinear CAD software is used for optimization of the "approximate" multiplier design presented in Section III. The approximate calculations for transistor bias and output termination obtained in Section III are used a starting point for CAD. Specifically, a ×2 6–12-GHz frequency multiplier using the NEC NE9000 FET is considered. The simplified schematic representing the multiplier used for the CAD simulations in Section IV is shown in Fig. 4.

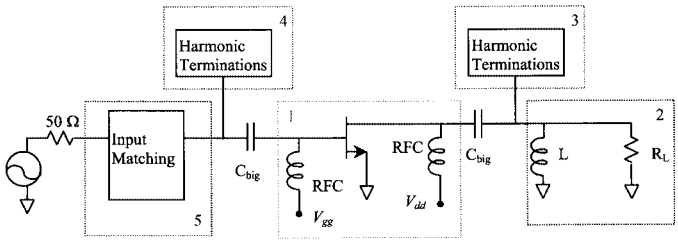

Fig. 4. Simplified multiplier schematic for CAD simulations.

Various design goals could be important, including maximizing output power, maximizing conversion gain, maximizing bandwidth, minimizing output distortion, or maximizing power efficiency, and would depend on the design requirements (keeping in mind, of course, that many of these are conflicting and cannot generally be obtained simultaneously). In this example, the multiplier is optimized to deliver maximum output power at 12 GHz.

Regardless of the ultimate design goal, a reliable multiplier design procedure usually involves effectively controlling the drain current harmonics. This objective seems simple enough, but is actually quite difficult since almost every portion of the circuit shown in Fig. 4 has an effect, and often a dramatic effect, on the drain current and its harmonic content. Although CAD optimization to obtain a desired goal is very powerful, it also tends to be somewhat erratic in producing a good solution if one attempts to optimize too many factors simultaneously. A procedure that consistently produces good results involves systematically optimizing small portions of the circuit to gradually obtain the desired performance. This approach maintains good control over the optimization, and is the one followed for the tutorial presentation.

The power of the CAD software for visualizing and understanding the nonlinear effects prevalent in FET multipliers, and also for optimizing critical design parameters, is demonstrated.

A. Transistor IV Curves

The transistor IV curves are useful to get an indication of potential performance of the FET as a multiplier. Parameters such as $I_{\max}$, $V_{g,\max}$, V_t, and $V_{\rm SAT}$, which were used in the rough design of the multiplier above, are directly available from the IV curves. Obtaining the IV curves is easy with *ADS*, using the nonlinear model for the device. In this example, the device is "cf_nec_NE900000_19930730," which uses the "eefet3" model. Press the "IV_curves.dsn" button to see the schematic for obtaining the IV curves.

Like a curve tracer, a "dc analysis" is specified, which sweeps the drain voltage for swept values of gate voltage (as specified by a "Parameter Sweep" block). A current probe element measures the corresponding drain current. Press "Simulate" to see the results.

The IV curves show the highly nonlinear nature of the device, particularly around the "saturation" and "pinchoff" regions, where reduction in transconductance is evident. The rough assumptions for $I_{\max}$, $V_{g,\max}$, V_t, and $V_{\rm SAT}$ are actually fairly consistent with the IV curves, with the exception of $I_{\max}$, which is approximately 115 mA at $V_{g,\max} = 0$ V, and slightly higher than assumed.

B. HB Simulation

The next step is to enter the rough starting parameters calculated in Section III and perform a nonlinear HB simulation. A seventh-order HB simulation is chosen and is likely accurate enough for the $\times 2$ multiplier. The order can be increased later if improved accuracy is desired. Press the "x2_mult_HB_init.dsn" button to see the schematic (portions 1 and 2 of Fig. 4) showing the initial multiplier parameters.

The time waveform measurements shown (i.e., "I_t," "V_t") require specification of appropriate node voltages and current probes and are available as a result of the inverse Fourier transform operation performed in the HB analysis. Access to the "nonsinusoidal" gate and drain time waveforms is extremely useful for visualizing and understanding the behavior of the multiplier, and also in verifying that the desired values for the critical design parameters shown in Fig. 2 (i.e., $I_{\max}$, $V_{g,\max}$, 2θ, $V_{\min}$, $V_{\max}$, etc.) are obtained.

For initial evaluation, no attempt to match a 50-Ω load impedance to that required at the drain of the multiplier is made, and the drain is terminated by the parallel inductance of 1.17 nH and resistance of 150 Ω, as calculated in Section III. Also, ideal biasing with large value blocking capacitors and feed inductors is assumed. These simplifications allow easier optimization of key parameters such as input level, gate bias, and termination impedances. Design of proper matching, termination, and biasing circuitry can be done at a later stage.

One parameter that is difficult to specify is the input level. From rough calculations in Section III, the desired peak gate voltage level is known, but its relationship to input drive level is not. Conjugate matching on the input is desired to maximize the conversion gain of the multiplier (defined as the harmonic power delivered to the load divided by the fundamental power available from the source, $P_{n,L}/P_{\rm avs}$), but since the load matching, termination, and biasing circuitry is yet unknown, and affects the input impedance of the FET, input matching at this stage is not practical and complicates the optimization. A more effective approach is to adjust the input level (which may be quite high due to mismatch) to maintain the desired gate voltage characteristics until optimization of the key parameters is complete, and then perform input matching at the end to recover the conversion gain. An initial guess of $P_{\rm avs} = +16$ dBm is used. Press "Simulate" to see the HB results with the initial multiplier parameters.

The simulation results look somewhat as expected, with a fairly sinusoidal gate voltage signal and a corresponding "clipped" drain current signal. The drain current reflects the phase shift from gate-to-drain, and the "soft" turn-on characteristic is also evident at low values. The maximum gate voltage is lower than required (-2 V versus 0 V), which results in a low maximum drain current (30 mA versus 100 mA), giving low output power and efficiency. The $P_{\rm avs}$ will have to be increased from $+16$ dBm to get the desired maximum gate voltage.

The drain voltage clearly reflects strong fundamental and second harmonic components (these are, in fact, comparable), which indicates that the simple parallel inductive susceptance does not have sufficiently high Q to adequately reject unwanted harmonics, particularly, the bothersome fundamental component, which is very large. It is evident that better harmonic short circuits are required at the drain. A simple short-circuit termination that works well for a doubler is an open-circuit $\lambda/4$ line at the fundamental frequency. This will short circuit the drain at the fundamental frequency and at odd harmonics, while remaining an open circuit, and not affect the second and even harmonics. Since even harmonics are quite low, this should "clean-up" the drain voltage waveform considerably. Press the "x2_mult_HB_oc_stub.dsn" button to see the addition of the open circuit $\lambda/4$ line, then press "Simulate" to see the effect.

Addition of the open circuit $\lambda/4$ line has effectively shorted the odd harmonics at the drain, leaving a drain voltage waveform composed primarily of the desired second harmonic. This technique, though simple, has its limitations for higher order multipliers ($\geq$ third order). In these cases, both the fundamental and second harmonic components are large, and should be shorted to ensure stability and low output distortion. Use of shorting stubs alone for both the fundamental and second harmonic is impractical since the reentrant nature of the stubs would invariably cause the desired harmonic to be shorted as well. A technique for achieving this seemingly contradictory objective is presented in Section V.

This objective can be satisfied by using ideal "harmonic terminations." This feature is purely a mathematical convenience, but allows termination of each harmonic in a specific impedance without affecting the other harmonics. This can be an extremely useful tool when choosing harmonic termination impedances for high harmonic multipliers. To illustrate this technique, the open-circuit termination is replaced by "harmonic terminations" in "x2_mult_HB_idlers.dsn" (added portion 3 of Fig. 4), which presents an open circuit at the second harmonic and short circuits at all other harmonics. Press the button to see how this is defined ("Push" into the "harm_term" block) and "Simulate" to see the effect in removing both the even and odd harmonic distortion.

The harmonic distortion has effectively been removed from the drain voltage. Distortion is also evident at the gate voltage, even at this low input level. The distortion is primarily second harmonic, and largely a result of the nonlinear gate-to-source capacitance. This effect may not be entirely undesirable, and can actually enhance the second-order nonlinearity in a $\times 2$ multiplier and increase the second harmonic drain current and output level. Large second harmonics, however, can leak out through the input port and can be problematic. For illustrative purposes, another "harm_term" block is added to the gate (added portion 4 of Fig. 4) to short the second harmonic. This could be realized using stubs or with the gate choke circuitry. The following section addresses the input bias and level.

1) Optimization of Bias and Level: The power of nonlinear CAD software is in optimization. Rough calculations produce a starting point for CAD, and manual tuning of key parameters is

difficult and very time consuming. Optimization, if done properly, can produce a realistic high-performance solution. However, one must keep in mind that the software does not know what the operator wants to accomplish, so the setting of optimization routines, goals, and variable parameters is critical, and takes practice and experience.

The gate input and bias level can be optimized to achieve a desired goal. Most likely, this goal will be to maximize a desired harmonic drain current component or harmonic power delivered to the load. Optimization for these goals tends to indirectly optimize drain current conduction angle, which would be difficult to specify directly as a goal due to the various influencing factors such as level, bias, and source and load terminations. Multiple goals can be specified, and, for this example, two goals are used. The first goal optimizes the "second" harmonic output power. The second goal restricts the gate voltage to 0 V maximum, allowing a fair comparison to the rough calculation in Section III. Press the "x2_mult_HB_opt_input.dsn" button to see how these are defined.

Since the maximum expected second harmonic output power from the rough calculations is 55 mW, the defined goal is set to a "min" of 50 mW and a "max" of 100 mW. "Gradient" optimization usually produces good results and is specified here. Gate bias voltage and input level are made variable in the optimization. Press "Optimize" to see the results of seven iterations of gradient optimization.

The results of the optimization show dramatic improvement in the performance. The second harmonic output power has increased to $+15.7$ dBm, and the maximum gate voltage is 0 V. The dc–RF efficiency has also become respectable at 28.8%. The conduction angle can be estimated from the markers and is approximately 125°, which is very close to the ideal value calculated in Section III. It is also interesting to look at how the input level and gate bias voltage have changed during the optimization. Press "Iterations" to see the values at each iteration.

The optimal input level and bias voltage are found very quickly and, in fact, the gradient optimization terminates with zero gradient after only four iterations. It is evident that the optimizer has adjusted the values for optimal conduction angle by increasing the level and shifting the bias voltage slightly lower, while maintaining a maximum gate voltage of 0 V.

2) Optimization of Output Termination: The next optimization is of the second harmonic output termination to obtain maximum output power. The gate voltage and input level are removed from the optimization, as is the gate maximum voltage goal. The optimization variables used now are the load inductance and resistance. The load inductance should resonate out the drain-to-source capacitance, while maximizing the second harmonic load current. The load resistance should be large enough to cause maximum drain voltage swing and maximize output power and efficiency. Press the "x2_mult_HB_opt_output.dsn" button to see how this optimization is defined and then press "Optimize."

Press the "x2_mult_HB_opt_output2.dsn" button to see the updated optimization values.

The load inductance and resistance values have changed somewhat from the rough calculation values. In particular, a larger load resistance (193 Ω versus 150 Ω) was required to saturate the drain voltage. After optimization, the second harmonic output power has increased to $+16.1$ dBm, and the dc–RF efficiency has increased to 31.8%. These values are quite respectable, compared to the rough calculation values of Section III.

The cause of the slight decrease in output level (16.1 versus 17.4 dBm) is a slight decrease in second harmonic load current. One can assume from the larger load resistance that the second harmonic load current has decreased to $(150/193) * 27 = 21$ mA. This can be confirmed from the optimization results above, as the second harmonic load current is available from the HB analysis (I_Probe2.i) and is equal to 21 mA. One explanation for the decrease in load current is likely an imperfect output resonator (i.e., the output admittance of the drain is more complicated than a simple capacitive susceptance). Another cause for the decrease is the nonlinear drain current waveform itself. The expected load current of 27 mA was calculated as the second harmonic of an ideal clipped sinusoid, which the actual drain current clearly is not. The decrease in dc–RF efficiency is also easily explained. Since the output level is 74% of the ideal and the dc current is higher, approximately by the ratio of $I_{\max}$ (i.e., $120\ \text{mA}/100\ \text{mA} = 1.2$), then the efficiency is decreased from 50% to approximately $50 * 0.74/1.2 = 31\%$.

3) Input Matching: Conjugate matching at the fundamental frequency must be done at the input to maximize the conversion gain of the multiplier. Various lumped and distributed matching circuits may be used to obtain the desired matching impedance at the fundamental frequency. These different circuits, however, may produce considerably different multiplier performance since they could provide dramatically different impedances to the other harmonics. In this tutorial example, the gate has been shorted at all harmonics, except the fundamental, so variability in matching circuit performance will be minimal.

One must be careful to maintain the gate voltage waveform as close as possible to the peak value obtained above (i.e., with $P_{\text{avs}} = +19.8$ dBm and no input matching). If this is neglected, difficulties may result when optimizing matching circuits since the matching greatly affects the gate voltage level and, thus, the output level. For illustrative purposes in this example, a lumped "L-type" reactive matching network is used.

Large-signal S-parameters (LSSP) are useful for estimating Γ_{in}. Once Γ_{in} is obtained, $\Gamma_S = \Gamma_{in}^*$ is set as a starting point for the optimization. For this example, with $P_{\text{avs}} = +19.8$ dBm, the required $\Gamma_S = 0.983\angle 44.5°$ (which is obtained ideally with series and shunt inductors of 13.2 and 4.3 nH). This illustrates potential problems in obtaining the conjugate match, as the input impedance is essentially reactive. It is, therefore, likely that one will have to settle for something less than maximum conversion gain.

Optimization of the input match with too many variables is very difficult, and it is best to only optimize one or two and iterate with trial and error. The approach taken here is to make the matching circuit elements variable and optimize for fixed input levels, gradually decreasing the level until a suitable gate voltage can no longer be obtained. The goal defined is to maintain the second harmonic output level near $+16.1$ dBm, as obtained above. Press the "x2_mult_HB_opt_input2.dsn" button

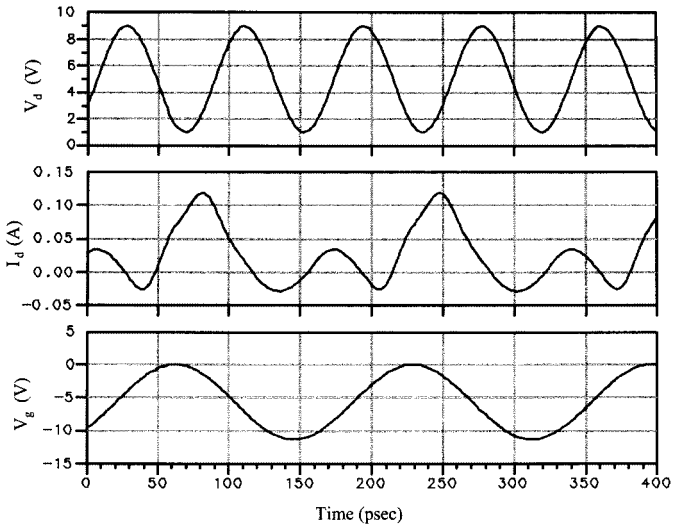

Fig. 5. Final gate and drain time waveforms for the multiplier example.

to see the circuit (added portion 5 of Fig. 4) and the optimization definition and then press "Optimize" to see the results.

After optimization, it is found that the input level can be decreased to +9 dBm, from +19.8 dBm, which results in a recovery of 10.8 dB of conversion gain from the highly mismatched situation. The inductor values are now 13.3 and 4.6 nH, a slight change from the nominal values. The second harmonic output power has been maintained at +16.1 dBm, and the dc–RF efficiency has also remained at 31.8%. The conversion gain of the multiplier is 7.1 dB, which is quite high, and one of the attractive features of active multipliers. The final gate and drain time waveforms for the multiplier example (with all portions of Fig. 4 included and optimized) are shown in Fig. 5. These are quite consistent with the time waveforms of Fig. 2 and the approximate parameters calculated in Section III.

The next step in the design would be to design realistic circuitry for the output matching, and harmonic termination circuitry, and optimize further to obtain a more accurate solution. This is not as difficult for a $\times 2$ multiplier as for higher harmonic multipliers and will not be demonstrated for the example $\times 2$ multiplier. Instead, an effective technique for designing the output circuitry for higher order multipliers is presented in Section V.

V. Output Circuit Considerations for High Harmonic Multipliers

As mentioned earlier, design of effective output termination circuitry is difficult for high harmonic multipliers, partly because the levels of unwanted low-order harmonics are high compared to the desired harmonic (as evidenced by Fig. 3) and partly due to the conflicting reentrant nature of shorting stubs at even and odd harmonics (i.e., want shorts at both evens and odds). The objective, therefore, is to design output circuitry that simultaneously provides optimal impedance at the desired harmonic to maximize output power, provides sufficient rejection of unwanted harmonics, and provides short-circuit terminations to unwanted harmonics at the FET drain to ensure stability. The later two objectives perhaps seem similar, but they are, in fact,

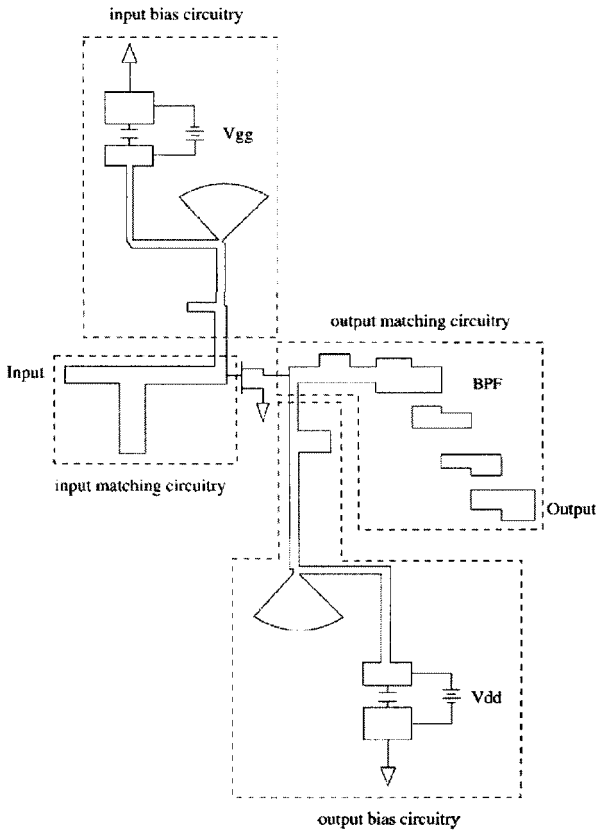

Fig. 6. Layout of $\times 4$ 28-GHz multiplier.

considerably different. Open-circuit terminations at the drain will also give high harmonic rejection at the output, but will result in large drain voltage variation and potential instability.

A technique for simultaneously obtaining these objectives is illustrated by way of example for a $\times 4$ output stage operating at 28 GHz. This design is based on the NEC NE1280 medium power heterojunction FET (HJ-FET) chip, and follows the procedure outlined in Sections III and IV of the tutorial. The drain of the FET is initially terminated using the ideal "harmonic terminations" technique described in Section IV-B. The gate-bias voltage and input level are adjusted, with all harmonics terminated in ideal short-circuit terminations ($\Gamma_n = 1\angle 180°$) until the desired maximum drain current and conduction angle is obtained. In this case, the optimal conduction angle (see Fig. 3) for the $\times 4$ is small (61°) and difficult to realize in the FET so a larger conduction angle (96°) is used. The termination impedance for the fourth harmonic is then optimized to produce maximum output power, while keeping the other harmonics terminated in short circuits. The optimal fourth harmonic reflection coefficient is found to be $\Gamma_4 = 0.81\angle 164°$.

Circuitry, shown in Fig. 6, to achieve this difficult harmonic termination objective is realized as a combination of a coupled-line bandpass filter at the fourth harmonic frequency, a section of 50-Ω transmission line, a stub matching circuit, and the drain bias choke. The bandpass filter provides rejection of unwanted harmonics at the output. An additional advantage in using a coupled-line filter is that it provides dc blocking for the drain bias and removes the requirement for a blocking capacitor,

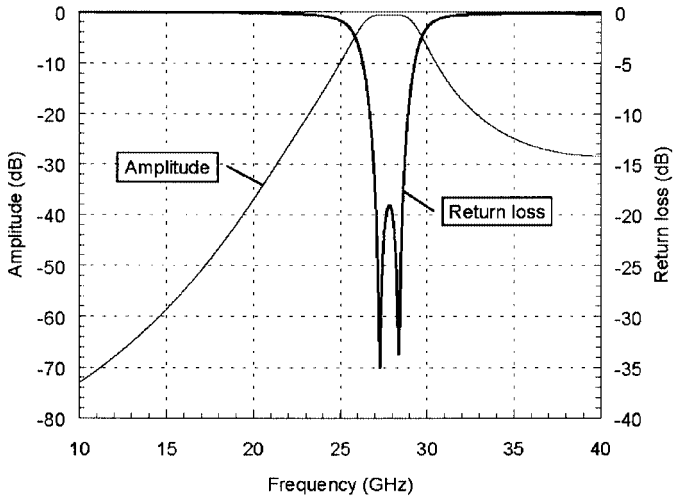

Fig. 7. Response of 28-GHz coupled-line bandpass filter.

TABLE I
DRAIN CHOKE AND COMBINED OUTPUT TERMINATION REFLECTION COEFFICIENTS FOR ×4 28-GHz MULTIPLIER

Harmonic	Freq. (GHz)	Γ_{choke}	Γ_L
1	7	0.98∠-172°	0.97∠-178°
2	14	0.99∠0°	0.99∠179°
3	21	0.92∠177°	0.94∠-172°
4	28	0.94∠0°	0.81∠164°

which is difficult to realize at 28 GHz. The filter used here is a second-order Butterworth filter, which provides adequate rejection and a 50-Ω impedance at 28 GHz that can be transformed to the desired fourth harmonic drain impedance. The filter response is shown in Fig. 7.

It is apparent from Fig. 7 that the bandpass filter has a well-matched passband at 28 GHz and substantial rejection at the first and second harmonic frequencies, which have the largest drain current components. As the return loss is near 0 dB, the impedance at harmonics other than the fourth is essentially reactive and the magnitude of the reflection coefficient is near one. As a result, a section of 50-Ω transmission line can be used to transform a reactive harmonic impedance to a short circuit at the FET drain, while having little effect on the 50-Ω impedance at 28 GHz, which can be transformed to the desired impedance with the reactive tuner. The lengths of the transmission line and tuning stubs are varied to obtain an effective drain short circuit at the second harmonic while simultaneously providing the desired impedance at the fourth harmonic. The short circuit at the fundamental and other odd harmonics is provided by the drain bias choke. The choke consists of a high-impedance feed line and a combination of radial and tuning stubs optimized to provide good short circuits at the fundamental and third harmonic.

The reflection coefficients of the drain bias choke and the load, as seen by the drain with the combined termination effects, is shown in Table I for various harmonic frequencies. This demonstrates that the desired fourth harmonic reflection coefficient has been obtained, while realizing near short circuits at all the lower order harmonics.

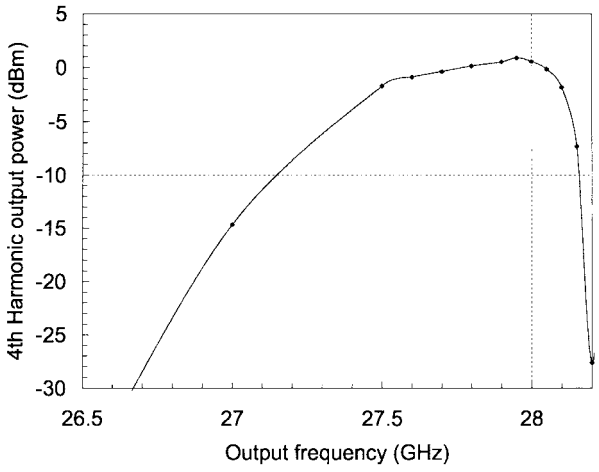

Fig. 8. Output power of ×4 multiplier.

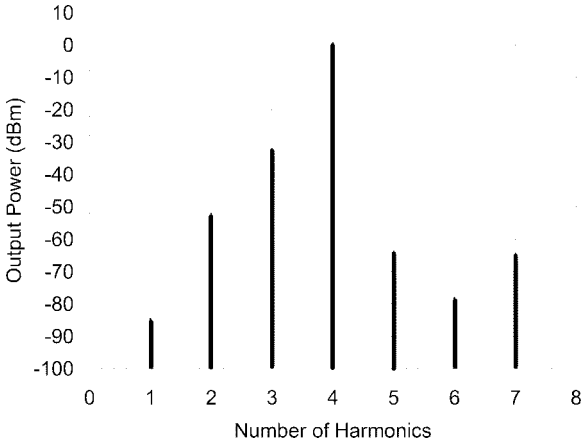

Fig. 9. Output spectrum of ×4 multiplier.

The output power as a function of frequency is shown in Fig. 8 for the ×4 multiplier with an input level of +5 dBm. Using the tutorial procedure, very good performance is obtained, as the multiplier provides +1-dBm output power at 28 GHz and a bandwidth of 500 MHz. The conversion gain (loss) is −4 dB, and quite good for a high-order multiplier. Fig. 9 shows the output spectrum of the ×4 multiplier. The termination approach presented is very effective in the design of the high-order multiplier, as the levels of undesired harmonic components are below 32 dBc. The large first and second harmonic components in particular have been attenuated dramatically, and are below 50 dBc.

VI. CONCLUSION

Active frequency multipliers are attractive circuits for emerging applications at upper microwave and millimeter-wave frequencies. Nonlinear CAD software employing HB is a powerful tool for accurate and effective realization of frequency multipliers. Particularly useful is the ability to view nonlinear voltage and current time waveforms at the FET gate and drain, vary gate voltage bias and level to optimize drain conduction angle, and design effective harmonic termination circuitry, which is especially important for high-order frequency multipliers where proper termination is critical for achieving optimal performance.

It is hoped that this tutorial paper has served as a useful introduction to some of the important parameters, considerations, and tradeoffs involved in high-order active frequency-multiplier design using CAD software. It is also hoped that the reader might consider the use of frequency/phase multipliers in future designs.

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